CLAIMS

1. (Currently Amended) Interfacing circuitry for transferring data from a first domain to a second domain, wherein the first domain is synchronized to a first clock and the second domain is synchronized to a second clock, the interfacing circuitry comprising:

a first storage component configured for temporarily storing one or more data bits and a valid bit, the first storage component being synchronized to the first clock;

a first multiplexer component connected to the first storage component for providing one or more data bits and a valid bit thereto and for receiving one or more data bits and a valid bit therefrom, coupled to the first domain for receiving one or more data bits and a valid bit therefrom, and controlled by a first Write_enable signal from the first domain, wherein the first Write_enable signal determines whether the first storage component keeps its current data and valid bit or latches in a new data and a new valid bit;

a second storage component configured for temporarily storing one or more data bits and a valid bit, the second storage component being synchronized to the second clock; and

a second multiplexer component connected to the second storage component for providing one or more data bits and a valid bit thereto and for receiving one or more data bits and a valid bit therefrom, coupled to the first storage component for receiving one or more data bits and a valid bit therefrom, and controlled by a second Write_enable signal from the second domain, wherein the second Write_enable signal determines whether the ~~first~~ second storage component keeps its current data and valid bit or latches in a new data and a new valid bit.

2. (Original) The interfacing circuitry of Claim 1, wherein the first clock is faster than the second clock.

3. (Original) The interfacing circuitry of Claim 1, wherein the first clock is faster than the second clock, the interfacing circuitry further comprising:

a third storage component connected to the second storage component for receiving one or more data bits and a valid bit therefrom and coupled to the first domain for providing the one or more data bits and the valid bit thereto, the third storage component being synchronized to the second clock.

4. (Original) The interfacing circuitry of Claim 1, further comprising:

a third multiplexer component coupled to the second domain for receiving one or more data bits and a valid bit therefrom, connected to the first storage component for receiving one or more data bits and a valid bit therefrom, connected to the second multiplexer component for outputting one or more data bits and a valid bit thereto, and controlled by a first Control signal, the first Control signal determining whether data and a valid bit are transferred from the first domain to the second domain or from the second domain to the first domain, the first Control signal being generated by a master arbiter logic;

a fourth multiplexer component coupled to the first domain for receiving one or more data bits and a valid bit therefrom, connected to the second storage component for receiving one or more data bits and a valid bit therefrom, connected to the first multiplexer component for outputting one or more data bits and a valid bit thereto, and controlled by a second Control signal, the second Control signal determining whether data and a valid bit are transferred from the first domain to the second domain or from the second domain to the first domain, the second Control signal being generated by the master arbiter logic;

a first AND gate connected to the master arbiter logic for receiving the second Control signal, and connected to the second storage component for receiving a valid bit therefrom;

a first OR gate connected to the first AND gate for receiving an output signal therefrom, coupled to the first domain for receiving the first Write_enable signal, and connected to the first multiplexer component for providing a control signal thereto;

a second AND gate connected to the master arbiter logic for receiving the first Control signal, and connected to the first storage component for receiving a valid bit therefrom; and

a second OR gate connected to the second AND gate for receiving an output signal therefrom, coupled to the second domain for receiving the second Write_enable signal, and connected to the second multiplexer component for providing a control signal thereto.

5. (Original) The interfacing circuitry of Claim 1, wherein the first clock is faster than the second clock, the interfacing circuitry further comprising:

a third storage component connected to the second storage component for receiving one or more data bits and a valid bit therefrom and coupled to the first domain for providing the one or more data bits and the valid bit thereto, the third storage component being synchronized to the second clock;

a third multiplexer component coupled to the second domain for receiving one or more data bits and a valid bit therefrom, connected to the first storage component for receiving one or more data bits and a valid bit therefrom, connected to the second multiplexer component for outputting one or more data bits and a valid bit thereto, and controlled by a first Control signal, the first Control signal determining whether data and a valid bit are transferred from the first domain to the second domain or from the second domain to the first domain, the first Control signal being generated by a master arbiter logic;

a fourth multiplexer component coupled to the first domain for receiving one or more data bits and a valid bit therefrom, connected to the second storage component for receiving one or more data bits and a valid bit therefrom, connected to the first multiplexer component for outputting one or more data bits and a valid bit thereto, and controlled by a second Control signal, the second Control signal determining whether data and a valid bit are transferred from the first domain to the second domain or from the second domain to the first domain, the second Control signal being generated by the master arbiter logic;

a first AND gate connected to the master arbiter logic for receiving the second Control signal, and connected to the second storage component for receiving a valid bit therefrom;

a first OR gate connected to the first AND gate for receiving an output signal therefrom, coupled to the first domain for receiving the first Write_enable signal, and connected to the first multiplexer component for providing a control signal thereto;

a second AND gate connected to the master arbiter logic for receiving the first Control signal, and connected to the first storage component for receiving a valid bit therefrom; and

a second OR gate connected to the second AND gate for receiving an output signal therefrom, coupled to the second domain for receiving the second Write_enable signal, and connected to the second multiplexer component for providing a control signal thereto.

6. (Currently Amended) The interfacing circuitry of Claim 1, wherein the first multiplexer component comprises:

a third multiplexer component connected to the first storage component for providing one or more data bits thereto and receiving one or more data bits therefrom, coupled to the first domain for receiving one or more data bits therefrom, and controlled by [[a]] the first Write_enable signal from the first domain, wherein the first Write_enable signal determines whether the first storage component keeps its current data or latches in a new data; and

a fourth multiplexer component connected to the second storage component for ~~providing a valid bit thereto and~~ receiving a valid bit therefrom and for providing a valid bit to the first storage component, coupled to the second domain for receiving a valid bit therefrom, and controlled by a second ~~Write_enable~~ control signal from the second domain, wherein the second ~~Write_enable~~ control signal ~~determines whether~~ selects between the first storage component ~~keeps its~~ valid bit or ~~latches in~~ a new valid bit.

7. (Original) The interfacing circuitry of Claim 1, wherein the second clock is faster than the first clock.

8. (Original) The interfacing circuitry of Claim 1, wherein the first storage component and the second storage component are registers.

9. (Original) The interfacing circuitry of Claim 1, wherein the first storage component and the second storage component are flip-flops.

10. (Original) The interfacing circuitry of Claim 1, wherein the first multiplexer is configured to output the one or more bits received from the first domain when the first Write_enable signal is asserted.

11. (Currently Amended) The interfacing circuitry of Claim [[1]]6, wherein the third multiplexer is configured to output the one or more data bits received from the first storage component when the valid bit received from the first storage component is asserted.

12. (Currently Amended) The interfacing circuitry of Claim [[1]] 11, wherein the first clock is faster than the second clock.

13. (Original) Interfacing circuitry for transferring data from a first domain to a second domain, wherein the first domain is synchronized to a first clock and the second domain is synchronized to a second clock, the interfacing circuitry comprising:

a first storage component configured for temporarily storing one or more data bits and a valid bit, the first storage component being synchronized to the first clock;

a first multiplexer component connected to the first storage component for providing one or more data bits thereto and for receiving one or more data bits therefrom, coupled to the first domain for receiving one or more data bits therefrom, and controlled by a first Write_enable signal from the first domain, wherein the first Write_enable signal determines whether the first storage component keeps its current data or latches in a new data;

a second multiplexer component connected to the first storage component for providing a valid bit thereto and for receiving a valid bit therefrom, coupled to the first domain for receiving a valid bit therefrom, and controlled by the first Write_enable signal from the first domain, wherein the first Write_enable signal determines whether the first storage component keeps its current data or latches in a new data;

a second storage component configured for temporarily storing one or more data bits and a valid bit, the second storage component being synchronized to the second clock;

a third multiplexer component connected to the second storage component for providing one or more data bits thereto and for receiving one or more data bits therefrom, coupled to the first storage component for receiving one or more data bits therefrom, and controlled by a second Write_enable signal from the second domain, wherein the second Write_enable signal determines whether the first storage component keeps its current data or latches in a new data; and

a fourth multiplexer component connected to the second storage component for providing a valid bit thereto and for receiving a valid bit therefrom, coupled to the first storage component for receiving a valid bit therefrom, and controlled by a second Write_enable signal from the second domain, wherein the second Write_enable signal determines whether the first storage component keeps its current valid bit or latches in a new valid bit.

14. (Original) The interfacing circuitry of Claim 13, wherein the first clock is faster than the second clock.

15. (Original) The interfacing circuitry of Claim 13, wherein the first clock is faster than the second clock, the interfacing circuitry further comprising:

a third storage component connected to the second storage component for receiving one or more data bits and a valid bit therefrom and coupled to the first domain for providing the one or more data bits and the valid bit thereto, the third storage component being synchronized to the second clock.

16. (Original) The interfacing circuitry of Claim 13, further comprising:

a fifth multiplexer component coupled to the second domain for receiving one or more data bits therefrom, connected to the first storage component for receiving one or more data bits therefrom, connected to the second multiplexer component for outputting one or more data bits thereto, and controlled by a first Control signal, the first Control signal determining whether data and a valid bit are transferred from the first domain to the second domain or from the second domain to the first domain, the first Control signal being generated by a master arbiter logic;

a sixth multiplexer component coupled to the second domain for receiving a valid bit therefrom, connected to the first storage component for receiving a valid bit therefrom, connected to the second multiplexer component for outputting a valid bit thereto, and controlled by a first Control signal, the first Control signal determining whether data and a valid bit are transferred from the first domain to the second domain or from the second domain to the first domain, the first Control signal being generated by a master arbiter logic;

a seventh multiplexer component coupled to the first domain for receiving one or more data bits therefrom, connected to the second storage component for receiving one or more data bits therefrom, connected to the first multiplexer component for outputting one or more data bits thereto, and controlled by a second Control signal, the second Control signal determining whether data is transferred from the first domain to the second domain or from the second domain to the first domain, the second Control signal being generated by the master arbiter logic;

a eighth multiplexer component coupled to the first domain for receiving a valid bit therefrom, connected to the second storage component for receiving a valid bit therefrom, connected to the first multiplexer component for outputting a valid bit thereto, and controlled by a second Control signal, the second Control signal determining whether a valid bit is transferred from the first domain to the second domain or from the second domain to the first domain, the second Control signal being generated by the master arbiter logic;

a first AND gate connected to the master arbiter logic for receiving the second Control signal, and connected to the second storage component for receiving a valid bit therefrom;

a first OR gate connected to the first AND gate for receiving an output signal therefrom, coupled to the first domain for receiving the first Write_enable signal, and connected to the first and second multiplexer components for providing a control signal thereto;

a second AND gate connected to the master arbiter logic for receiving the first Control signal, and connected to the first storage component for receiving a valid bit therefrom; and

a second OR gate connected to the second AND gate for receiving an output signal therefrom, coupled to the second domain for receiving the second Write_enable signal, and connected to the third and fourth multiplexer components for providing a control signal thereto.

17. (Currently Amended) A method for asynchronously transferring data from a first domain to a second domain, wherein the first domain is synchronized to a first clock and the second domain is synchronized to a second clock, the method comprising the steps of:

receiving one or more data bits and a valid bit from the first domain;

temporarily storing the one or more data bits and the valid bit in the first domain;

waiting for the valid bit to be asserted;

latching in the one or more data bits to the second domain within one cycle of the second clock after valid bit is asserted; and

temporarily storing the one or more data bits and the valid bit in the second domain.

18. (Original) The method of Claim 17, further comprising the step of:

storing the one or more bits and the valid bit in the second domain for at least one cycle of the second clock after the valid bit is asserted; and

probing the one or more bits and the valid bit from the first domain to confirm the receipt of the one or more data bits and the valid bit by the second domain before transferring a new data from the first domain to the second domain.

19. (Original) The method of Claim 17, wherein the first clock is faster than the second clock.

20. (Original) The method of Claim 17, wherein the second clock is faster than the first clock.